DeSyRe

on-Demand System Reliability

Key innovation

The DeSyRe project performs research on the design of future reliable Systems-on-Chip (SoCs). These are systems that guarantee continuous and correct operation in the existence of different types of faults. It is a well known fact that various systems are extremely sensitive to faults; typical examples are medical embedded systems, in which a single malfunction will put the life of a patient in danger.

However, as semiconductor technology scales, chips are becoming ever less reliable; prominent reasons for this phenomenon are the sheer number of transistors on a given silicon area and their shrinking device features. As a consequence, fault tolerance, provided through various redundancy schemes, comes at an enormous increase in power and performance cost. To make matters worse, power-density is becoming a significant limiting factor for performance and SoC design in general. In the face of such changes in the technological landscape, current solutions for fault-tolerance are expected to introduce an excessive overhead in future SoCs.

At the increasing fault-rates, expected in the upcoming technology generations, *DeSyRe will develop new design techniques for future reliable SoCs.* The primary project objectives are to reduce, compared to existing approaches, the power and performance overheads of fault-tolerance by 10-20%, as well as to improve yield decreasing the number of defective chips by 10-40%. The developed techniques will be used to design new advanced embedded systems targeting future high-tech medical devices for new treatments.

Technical approach

The above will be achieved through the following main contributions:

Designing and manufacturing totally fault-free systems has a heavy even prohibitive impact in its cost and performance. Instead, in DeSyRe we will design fault-tolerant systems built out of unreliable components, rather than aiming at totally fault-free chips. Only a small fraction of a DeSyRe chip will be required to be **fault-free**; this fraction will, then, be assigned the critical task of monitoring and maintaining the correct operation of the remaining unreliable (**fault-prone**) chip-resources which are responsible for the main functionality of the SoC.

In addition, DeSyRe SoCs will be on-demand adaptive to various types and densities of faults, as well as to other system constraints and application requirements. For leveraging on-demand adaptation/ customization and reliability at reduced cost, DeSyRe will employ three abstraction layers: the **Runtime System** and **Middleware** software layers, running on the fault-free part of the SoC, and the **Components** layer, composing the fault-prone area of the chip. The DeSyRe Components will deliver the functionality of the targeted SoC and will be built on a new dynamically reconfigurable substrate to provide flexibility and adaptation. The Middleware layer will be responsible for the dynamic reconfiguration of the fault-prone (reconfigurable) area in order to adapt the system, isolate and correct faults. Finally, the Runtime System layer has the top-level overview of the system; it manages the on-chip resources based on the application requirements (e.g. performance, functionality) and the system constraints (e.g., available resources, types and densities of faults).

Demonstration and Use

DeSyRe will deliver a well-defined, generic, and repeatable design framework for a large variety of SoCs. The proposed framework will be applied to two **medical SoCs** with high reliability constraints and diverse performance and power requirements. The first one is a *portable artificial cerebellum* used for rescuing part of a biological brain, while the second one is an *implantable artificial pancreas* which measures the glucose concentration in the blood of a diabetic person and accordingly releases the proper amount of insulin.

Contract number

287611

Project coordinator

Chalmers University of Technology

Contact person

Ioannis Sourdis

CSE department

Chalmers University of Technology

Rännvägen 6, 41296

Göteborg, Sweden

Tel: +46 317721744

Fax: +46 317723663

sourdis@chalmers.se

Project website

www.desyre.eu

Community contribution to the project

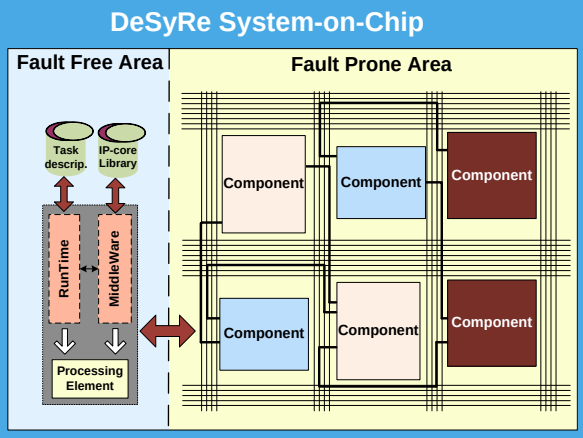
2.8 Million Euro

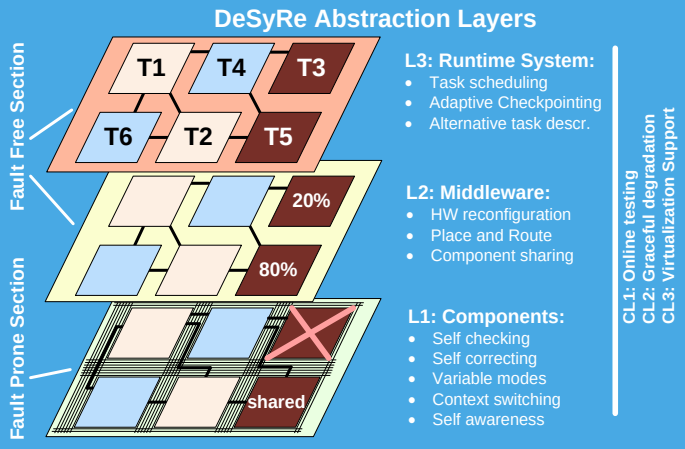
Project start date

1st October 2011

Duration

36 months





Scientific, Economic and Societal Impact

Developing new design techniques for more efficient customizable and adaptive systems has a clear market motivation on improving fault-tolerance, power-efficiency, and performance of future SoCs. This motivation is becoming stronger due to the changing technological landscape; chips are becoming less reliable while performance is severely limited by power consumption and heat dissipation. DeSyRe addresses the above challenges in order to enhance European competitiveness and increase market share in computing systems at the new technological landscape of 2015-2020.

DeSyRe brings together some of the leading European experts in the area. The presence of strong academic partners and competitive, rapidly growing industrial players in the consortium is expected to bring significant scientific and technological advances in the design of future SoCs. The SMEs of the project will exploit the various results produced in their respective domains; this is expected to strengthen their market position and competitiveness having a multiple returns on investment. The universities and research organizations will stay on the forefront of research in using the results. This will ultimately lead to new young European experts, trained in the new technologies developed in the project, as well as to new high technology jobs for European workers.

DeSyRe targets Fault-Tolerant SoCs primarily in the embedded domain. The impressive and ever-increasing penetration of embedded devices as well as the ubiquity demands made on such systems by modern society trends make this domain our primary focus. Considerable reductions of the energy and performance overheads for fault tolerance will contribute to more efficient embedded SoCs used in various activities of our everyday life. Within the project, new advanced medical systems will be prototyped achieving the first, crucial step towards the commercialization of future high-tech medical devices. Such medical devices will bring about new treatments and means to significant pathoses for the end-users.

Project partners	Country
Chalmers University of Technology	SE
University of Bristol	UK
EPFL	CH
FORTH	EL
Imperial College London	UK
Neurasmus BV	NL
Yogitech SpA	IT
Recore Systems BV	NL

Key Features

- **Scientific and Technological advances in the design of reliable future SoCs:**
  - 10-40% fewer defective chips
  - 10-20% lower energy cost for fault-tolerance
  - 10-20% lower performance overhead for fault-tolerance
- **Targeting new advanced embedded SoCs:**
  - future high-tech medical devices

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