DeSyRe
on-Demand System Reliability

Project Periodic Report for the first 6 months

CONTRACT NR	287611
TYPE OF DOCUMENT	Deliverable D1.3.1
AUTHOR	All WP leaders
ABSTRACT	Project Periodic Report for the first 6 months.
WORKPACKAGE	WP1
DESSEMINATION LEVEL	Restricted

DOCUMENT HISTORY

Release	Date	Comments	Status	Distribution
v0.1	06-04-2012	Initial draft, Integrating contributions from all WPs	draft	All Partners
v0.2	26-04-2012	The project management and use of resources sections were added	draft	All Partners
v0.3	27-04-2012	First complete draft, Section 1 included	draft	All Partners
v0.4	30-04-2012	text modifications	draft	All Partners
v0.5	30-04-2012	Incorporating final comments	draft	All Partners
v1.0	01-05-2012	Finalization of the report	final	EC

PROJECT PERIODIC REPORT

Grant Agreement number: 287611

Project acronym: DESYRE

Project title: on-Demand System Reliability

Funding Scheme: FP7-ICT-2011-3.4

Date of latest version of Annex I against which the assessment will be made:

Periodic report: 1st ☑ 2nd ☐ 3rd ☐ 4th ☐

Period covered: from 1st October 2011 to 31st March 2012

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[1] Usually the contact person of the coordinator as specified in Art. 8.1. of the Grant Agreement .

[2] The home page of the website should contain the generic European flag and the FP7 logo which are available in electronic format at the Europa website (logo of the European flag: http://europa.eu/abc/symbols/emblem/index_en.htm logo of the 7th FP: http://ec.europa.eu/research/fp7/index_en.cfm?pg=logos). The area of activity of the project should also be mentioned.

Declaration by the scientific representative of the project coordinator

I, as scientific representative of the coordinator of this project and in line with the obligations as stated in Article II.2.3 of the Grant Agreement declare that:

- The attached periodic report represents an accurate description of the work carried out in this project for this reporting period;
- The project (tick as appropriate) [3]:
  - ☑ has fully achieved its objectives and technical goals for the period;
  - ☐ has achieved most of its objectives and technical goals for the period with relatively minor deviations.
  - ☐ has failed to achieve critical objectives and/or is not at all on schedule.
- The public website, if applicable
  - ☑ is up to date
  - ☐ is not up to date
- To my best knowledge, the financial statements which are being submitted as part of this report are in line with the actual work carried out and are consistent with the report on the resources used for the project (section 3.4) and if applicable with the certificate on financial statement.
- All beneficiaries, in particular non-profit public bodies, secondary and higher education establishments, research organisations and SMEs, have declared to have verified their legal status. Any changes have been reported under section 3.2.3 (Project Management) in accordance with Article II.3.f of the Grant Agreement.

Name of scientific representative of the Coordinator: .....Ioannis Sourdis.....

Date: ...../ ...../ .....

For most of the projects, the signature of this declaration could be done directly via the IT reporting tool through an adapted IT mechanism.

[3] If either of these boxes below is ticked, the report should reflect these and any remedial actions taken.

Contents

1. Publishable Summary

Project Name:	**On-Demand System Reliability**
Project Acronym:	**DeSyRe**
Project Promo Images:	
Project's Official Website:	http://www.desyre.eu/
Project Type and Reference:	**FP7-ICT- 287611**
Project Duration:	**36 months** (start date: 1st Oct 2011)
Total Budget:	**€ 3.567.136** (including own contribution)
Project Co-ordinator:	Dr. Ioannis Sourdis Computer Science and Engineering dept. Chalmers University of Technology, Sweden Tel: +46 (0) 31-772 17 44 Fax: +46 (0) 31-772 36 63 E-mail: sourdis@chalmers.se

DeSyRe Consortium		
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Chalmers University of Technology		Sweden
University of Bristol		United Kingdom
Ecole Polytechnique Federale de Lausanne		Switzerland
Foundation for Research and Technology Hellas		Greece
Imperial College of Science, Technology and Medicine		United Kingdom
Neurasmus B.V.		The Netherlands
Yogitech SpA		Italy
Recore Systems B.V.		The Netherlands

This document presents the main results achieved in the DeSyRe project during the first 6 months of the project.

1.1 Summary description of the project

DeSyRe performs research on the design of future reliable Systems-on-Chip (SoCs). These are systems that guarantee continuous and correct operation in the existence of different types of faults. It is a well known fact that various systems are extremely sensitive to faults. Typical examples are medical (i.e. implantable cardiac pacemakers) or automotive systems (i.e. vehicle stability control), in which the shortest stop in operation will cause dramatic damages. Therefore, such applications require a fault-tolerant system, which guarantees correct and reliable functioning at any time.

However, as semiconductor technology scales, chips are becoming ever less reliable; prominent reasons for this phenomenon are the sheer number of transistors on a given silicon area and their shrinking device features. As a consequence, fault tolerance, e.g. provided through various redundancy schemes, has an enormously increasing power and performance cost. To make matters worse, power-density is becoming a significant limiting factor for performance and SoC design in general. In the face of such changes in the technological landscape, current solutions for fault-tolerance are expected to introduce an excessive overhead in future SoCs. Attempting to design and manufacture a totally fault-free system, would impact heavily, even prohibitively, the design, manufacturing, and testing costs, as well as the performance and power consumption of a system.

DeSyRe builds new, more efficient, adaptive fault-tolerant SoCs delivering a new generation of by design, on-demand reliable systems. Compared to existing approaches, the DeSyRe objective is to reduce the power and performance overheads of fault-tolerance by 10-20%, as well as to improve yield by decreasing the number of defective chips by 10-40%.

The above will be achieved through the design of fault-tolerant systems built out of unreliable components, rather than aiming at totally fault-free chips. DeSyRe systems will be on-demand adaptive to various types and densities of faults, as well as to other system constraints and application requirements. For leveraging on-demand adaptation/customization and reliability at reduced cost, a new dynamically reconfigurable substrate is designed and combined with runtime system software support. The developed design will be applied in two medical SoCs with high reliability constraints and diverse performance and power requirements.

The industrial beneficiaries of the project will exploit the various results of the project in their respective domains. It is expected that they will strengthen their market position and competitiveness having a multiple return on investment. The universities and research organizations will stay on the forefront of research in using the results. The project will strongly contribute in substantiating their prestige in the scientific community. The European citizens will benefit from cheaper hardware and lower power consumption of various consumer goods.

1.2 Overall Project Objectives

The DeSyRe proposal is motivated by the current **technology and business trends in microelectronics**. As semiconductor technology scales, chips are becoming less reliable, increasing the cost of building fault-free systems. Furthermore, increasingly more microelectronics suppliers spin-off their semiconductor divisions and become fabless to avoid the excessive fabrication costs, but -as a consequence- they also release control of their devices' reliability.

In response to the above technology and business trends, the primary aim of DeSyRe is to **define a generic design framework for fault-tolerant heterogeneous MPSoCs at reduced cost.** The developed framework will be applied to two medical systems. More precisely, DeSyRe has the following four research objectives:

Obj. 1. **Reliability at reduced cost:** DeSyRe will deliver systems tolerant to permanent, intermittent and transient faults at reduced power and performance overhead compared to existing solutions. (Project Object 1 will be achieved in milestone 6.1 in month 36)

Obj. 2. **On-demand adaptive systems:** The proposed design framework will deliver systems built on flexible/reconfigurable hardware substrate with runtime system mechanisms and virtualization support to on-demand adapt their configuration to:

- **Faults:** different fault rates and fault types (permanent, intermittent, transient)
- **System constraints:** available energy, maximum power, available resources etc., and
- **Application Requirements:** real-time performance, required fault tolerance level etc.

(Project Object 2 will be achieved in milestone 6.1 in month 36)

Obj. 3. **Reliable by Design:** attempting to provide fabless companies with the means to **guarantee the reliability of their products by design**, the proposed DeSyRe design framework aims at being (to some extent) **technology-independent**, providing **reliable systems containing unreliable components**. Within certain bounds, the defect-rates of a specific manufacturing process and technology will affect only the power consumption and performance of a system, rather than its correct operation. DeSyRe will provide mechanisms to support essential system attributes such as:

- **graceful degradation,**
- **online testing,**
- **virtualization,**
- **error detection, fault isolation, error correction and retry,**
- **self-checking and self-repairing.**

(Project Object 3 will be achieved in milestone 6.1 in month 36)

Obj. 4. **Increased Defect tolerance:** the flexibility of reconfigurable hardware will be exploited in order to **cope with permanent faults** (design, manufacturing, and due to aging faults); as a consequence DeSyRe SoCs will have:

- **increased manufacturing yield** by tolerating more manufacturing faults.
- **longer SoC lifetime** by tolerating more defects due to aging.
- **reduced manufacturing cost:** tolerating a larger number of manufacturing defects can lower the defect density standards of the manufacturing process and consequently reduce its cost.
- **shorter time to market:** tolerating more design faults can reduce the number of iterations required until a new, correctly-functioning SoC is produced.

(Project Object 4 will be achieved in milestone 6.1 in month 36)

1.3 Expected final results and their impact and use

1.3.1 Expected final results of the project

The expected measurable and verifiable outcomes of the project will be the following:

- The description of the **generic, structured, and repeatable DeSyRe design framework for reliable heterogeneous systems on chip**. The developed methods and techniques will deliver **adaptive systems** built on a **dynamically reconfigurable underlying hardware** and supported by **runtime system optimizations** to fit system's conditions and meet application requirements, such as available energy, maximum power consumption, real-time performance constraints, required fault-tolerance levels, number and type of faults which occur in the system (related to **objectives 1, 2 and 3**).
- The DeSyRe framework will be applied to two **medical SoCs** both having high reliability requirements, but diverse power and performance constraints. As a proof of concept, working (functionally correct) instances of the DeSyRe-based above SoCs will be **prototyped on FPGA** integrating the techniques developed during the project (related to **objectives 1, 2 and 3**).
- A DeSyRe SoC is expected to be **tolerant to transient, intermittent and permanent faults at reduced energy and performance overhead compared to existing approaches for fault tolerance.** At the end of the project, the DeSyRe framework will be evaluated and compared to existing solutions. The energy, performance, and area cost for providing a reliable system will be measured in the existence of various fault types and fault rates (related to **objective 1**). Compared to a triple-modular-redundancy (TMR) scheme, we expect that DeSyRe will deliver techniques with:
    - up to 10% reduction in energy for tolerating transient faults, while in the case of intermittent faults the reduction can be up to 20%.
    - The area or performance costs depend on the design choice for redundancy in space or in time, respectively. The reduction in area or performance overhead is expected to be 10-20%.
    - The expected improvements on tolerating permanent faults (defects) are discussed below.
- SoCs that follow the DeSyRe framework are expected to have **increased defect tolerance** compared to previous related works (related to **objective 4**). Compared to redundancy at the core-level, a DeSyRe MPSoC is expected to deliver:
    - **better manufacturing yield:** as our approach is expected to **tolerate more defects, the**n given a fixed defect rate, a higher percentage **of the manufactured chips will be functioning** correctly. The DeSyRe approach is expected to reduce the defective chips by 10-40%.
    - **10-40% longer SoC lifetime (Mean-Time-To-Failure / MTTF):** providing better defect tolerance, our solution will be able to more efficiently cope with aging effects and lengthen SoCs lifetime for a given error rate density, distribution (in time and space).
    - **lower manufacturing cost:** the manufacturing process will no longer need to deliver totally fault-free chips, and hence will be less expensive.
    - **shorter Time-to-Market: be**ing more defect-tolerant, and thus tolerant in design defects, a chip will require fewer iterations during the **manufacturing process in orde**r to deliver a SoC that fulfils the expected requirements.

1.3.2 Impact

Developing new design techniques for more efficient customizable and adaptive systems has a clear market motivation on improving fault-tolerance, power-efficiency, and performance of future SoCs. This motivation is becoming stronger due to the changing technological landscape; chips are becoming less reliable while performance is severely limited by power consumption and heat dissipation. DeSyRe addresses the above challenges in order to enhance European competitiveness and increase market share in computing systems at the new technological landscape of 2015-2020.

DeSyRe brings together some of the leading European experts in the area. The presence of strong academic partners and competitive, rapidly growing industrial players in the consortium is expected to bring significant scientific and technological advances in the design of future SoCs. The SMEs of the project will exploit the various results produced in their respective domains; this is expected to strengthen their market position and competitiveness having a multiple returns on investment. The universities and research organizations will stay on the forefront of research in using the results. This will ultimately lead to new young European experts, trained in the new technologies developed in the project, as well as to new high technology jobs for European workers.

DeSyRe targets Fault-Tolerant SoCs primarily in the embedded domain. The impressive and ever-increasing penetration of embedded devices as well as the ubiquity demands made on such systems by modern society trends make this domain our primary focus. Considerable reductions of the energy and performance overheads for fault tolerance will contribute to more efficient embedded SoCs used in various activities of our everyday life. Within the project, new advanced medical systems will be prototyped achieving the first, crucial step towards the commercialization of future high-tech medical devices. Such medical devices will bring about new treatments and means to significant pathoses for the end-users.

1.3.3 Use

The consortium presents a balanced research effort between industrial partners, public research institutes and higher-education institutions. All partners have plans and possibilities for the exploitation of knowledge gained during the DeSyRe project. Our *Application partner* will complete the prototypes of their new advanced medical systems as the first step towards end-products. *Technology partners* will impact the market via the newly developed design techniques for future SoCs. *Academic partners* will also exploit the results of the project gaining new knowledge in the related fields and educating young researchers in the developed technologies.

The project is to explore a new dynamically reconfigurable substrate complimented with system-level software-layers to provide fault-tolerance at lower costs. At the end of the project we will conclude on the effectiveness of our approach and its costs in power, performance, and area, as well as on the complexity of managing such systems. This knowledge is essential to further explore and improve the proposed ideas towards building next-generation reliable and adaptive systems.

We will create solutions to improve reliability, safety, survivability and adaptiveness of future SoCs. As a consequence, we will open the way for new applications (medical, automotive, space, etc.) to exploit the developed technologies and build more efficient systems which will benefit society as a whole. Furthermore, reduced manufacturing costs and time-to-market as well as increased yield will free monetary resources that could, then, be redirected to other relevant topics. Last but not least, the general public will benefit from the advances provided by the end-user medical applications.

1.4 Overview of Work performed and Achievements in the first 6 months

Below, we give an overview of the technical work performed and the achievements in the project up to month 6:

- We have successfully finished the Requirements phase of the project. We described the requirements of the DeSyRe design framework. These requirements are currently used in the design phase which started in month 5 and will deliver the DeSyRe design techniques for future reliable Systems on Chip.
- We performed the (dependability) analysis of the two medical applications/systems considered in the project, namely the artificial cerebellum and the artificial pancreas. This analysis will be used in order to select a subset of the DeSyRe design techniques to be applied in each one of the two systems.
- We have an initial system architecture description, which is the starting point for the final DeSyRe System Architecture to be delivered at the end of the first year.
- We have a first version of the evaluation metrics, which will be refined when we define our evaluation methodology, in months 14-15. The evaluation metrics will be used at the end of the project to measure the effectiveness of the developed DeSyRe design techniques.

The above are the first steps towards the project objectives and expected final results of the projects as described in the previous sections and in the Description of Work.